

aP58Q7M/Q8M

38 / 76 minutes

Multi-time program voice 2 chip solution

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■ Part no. information

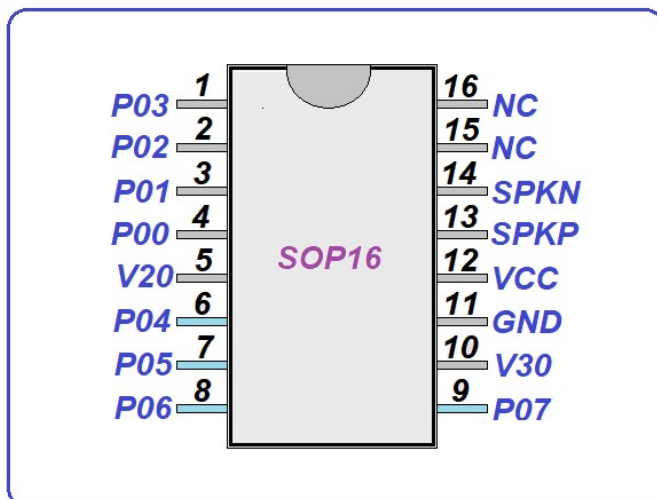
aP58QxM is combined part no. including aP58HQ and SPI flash, 2 chips

aP58Q7M = aP58HQ DSP + 64M SPI Flash

aP58Q8M = aP58HQ DSP + 128M SPI Flash

■ Features :

- Built in 8-bit DSP
- System CPU clock :24MHz
- Program memory : 512k bits(64 K Bytes) OTP.
- Voice memory : 64M/128M bits(8M/16M Bytes) FLASH memory
- 38/76 Min voice length at 5.8KHz sampling or 9.5/19 Min voice length at 23KHz sampling.
- Built-in 2k bits(256 Bytes) SRAM.
- Built-in R/C Trim (1%)
- Built-in 1 set PWM and 1 set DAC..
- GPIO x 4 available
- Built in low voltage detection and reset system circuit (LVR/LVD)
- Built-in Watch Dog Timer.
- Optional PWM driving ability : High Middle Low Buffer Drive .
- Operating Voltage Range: 2.3V ~ 5.0V.
- Five standard triggering modes are available
 - SBT mode
 - Matrix key
 - Cpu serial 1-wire mode
 - Cpu serial 2-wire mode
 - Cpu serial 3-wire mode



aP58HQ SOP16

■ PIN NAMES :

Pin No.	Designation	I/O	Description
1	P0[3] / Reset	I/O	Port-0 I/O or external reset
2	P0[2]	I/O	Port-0 I/O.
3	P0[1]	I/O	Port-0 I/O
4	P0[0]	I/O	Port-0 I/O
5	V20	P	Digital Power.
6	P04	I/O	Port-0 I/O.
7	P05	I/O	Port-0 I/O.
8	P06	I/O	Port-0 I/O
9	P07	I/O	Port-0 I/O
10	V30	P	IO Power.
11	GND	P	System Ground.
12	VCC	P	Chip Power.
13	SPK_P	O	DAC / PWM1
14	SPK_N	O	PWM2
15	NC		
16	NC		

Group Options :

Selectable options that affect each individual group are called Group Options. They are:
Edge or Level trigger.

Unholdable or Holdable

Re-trigger or Non-retrigger

Stop pulse disable or enable.

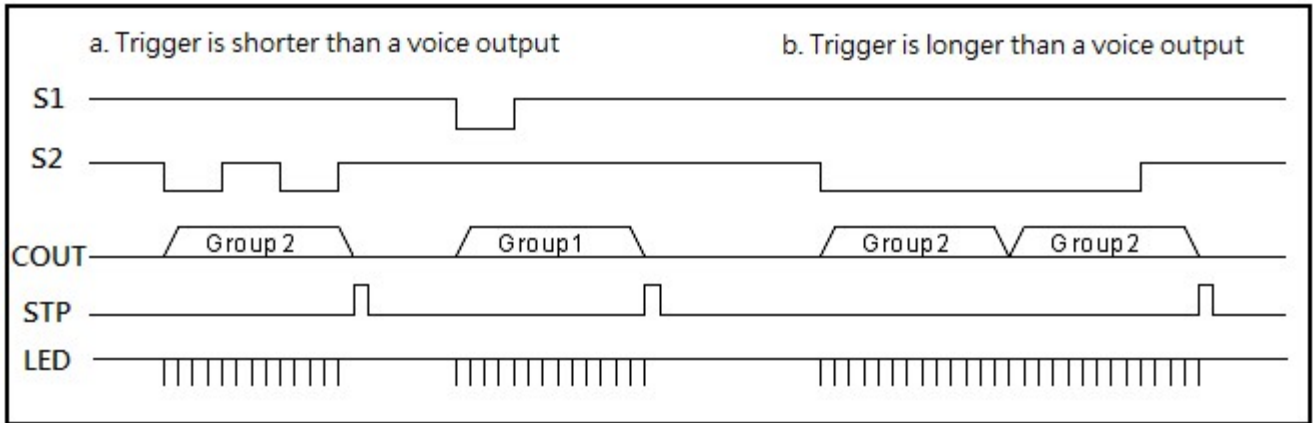


Fig. 1 Level, Unholdable, Non-retrigger

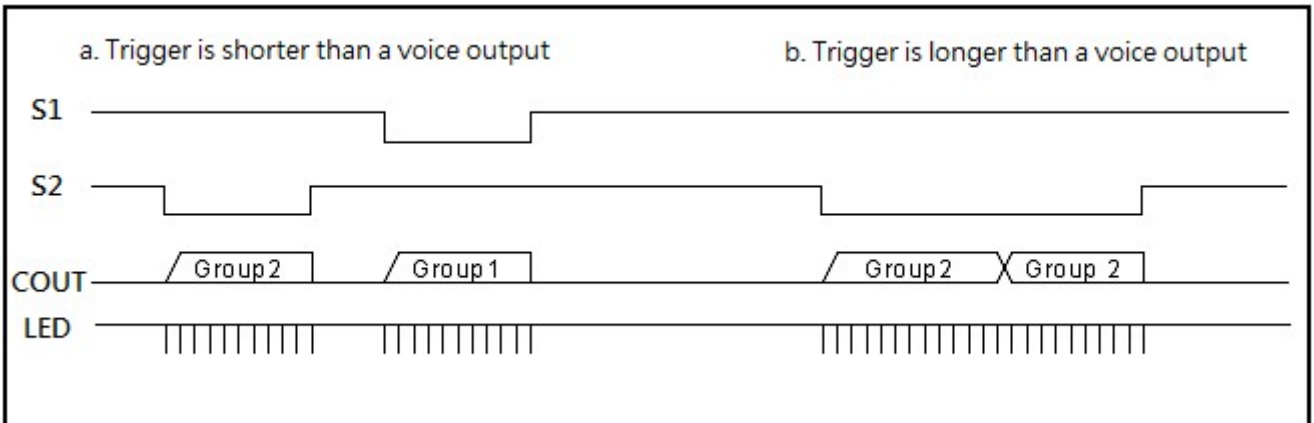


Fig. 2 Level Holdable

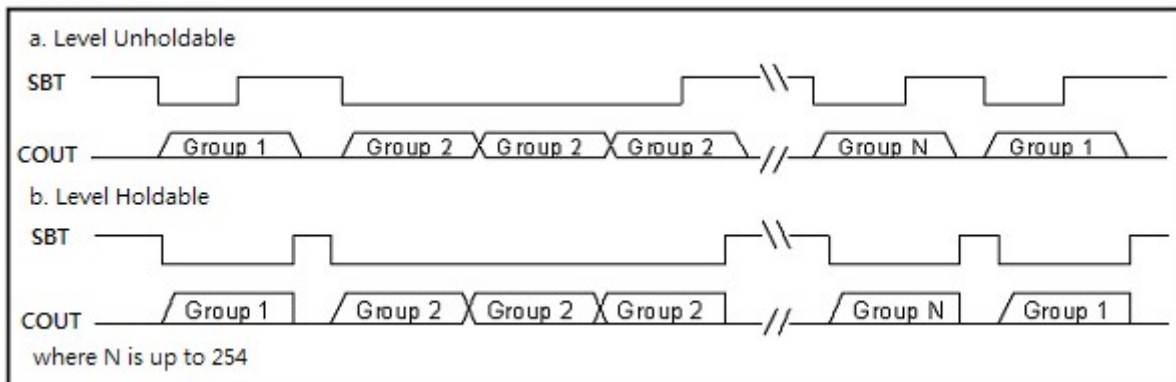


Fig. 3 SBT sequential trigger with Level Holdable and Unholdable

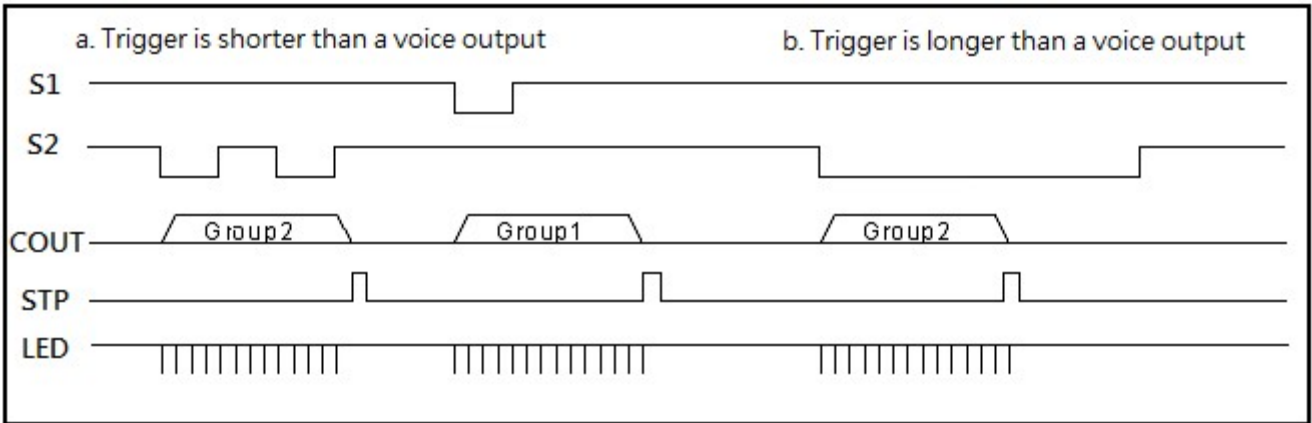


Fig. 4 Edge, Unholdable, Non-retrigger

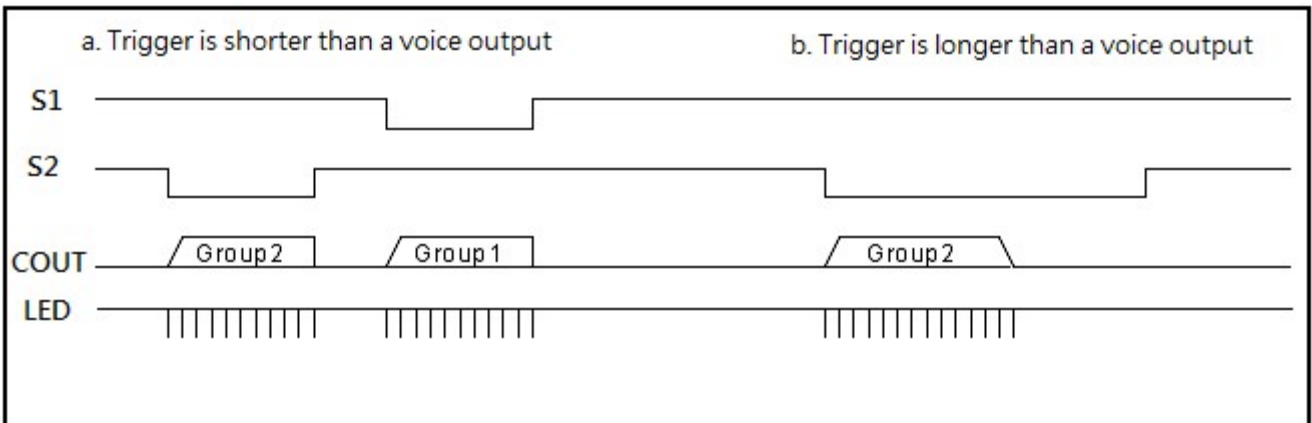


Fig. 5 Edge, Holdable

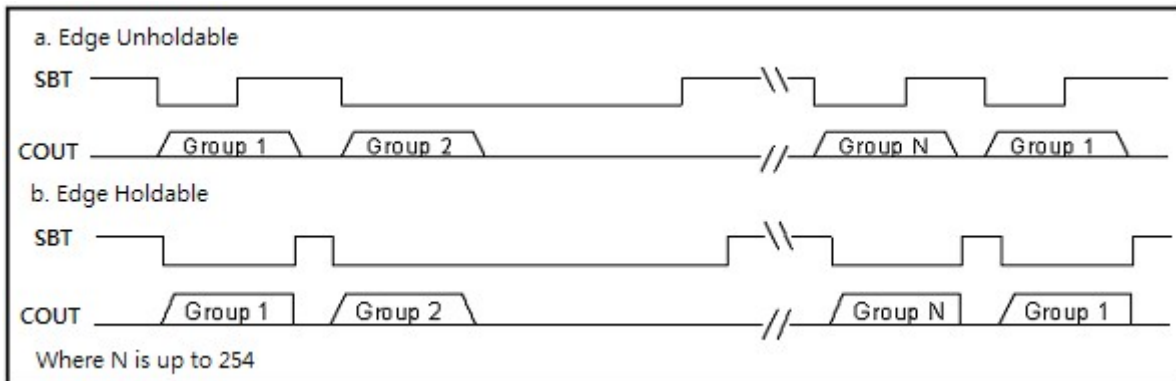


Fig. 6 SBT sequential trigger with Edge Holdable and Unholdable

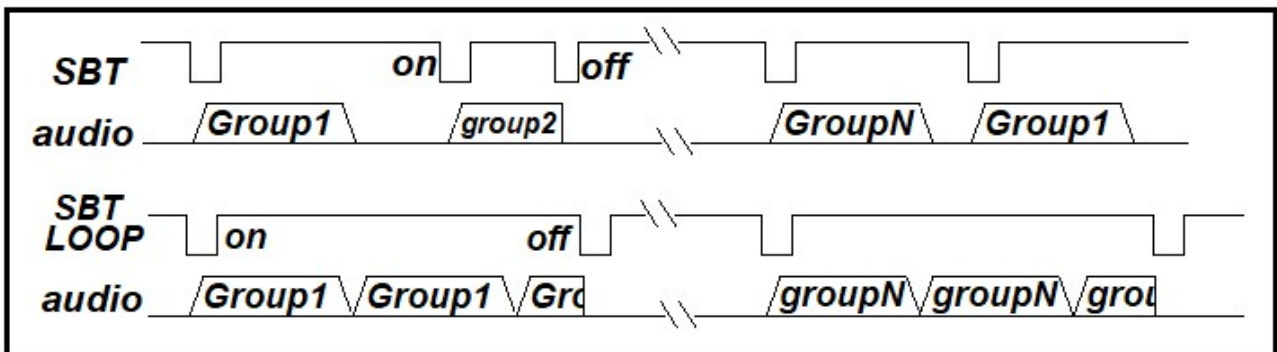


Fig. 7 SBT sequential trigger with On/Off

● **Trigger mode :**

1. **SBT mode :**

Maximum Voice Groups : 254 for each I/O. All I/O can be chosen input or output. Each Voice Group can have its independent trigger options (See Fig. 1,2,4 and 5).

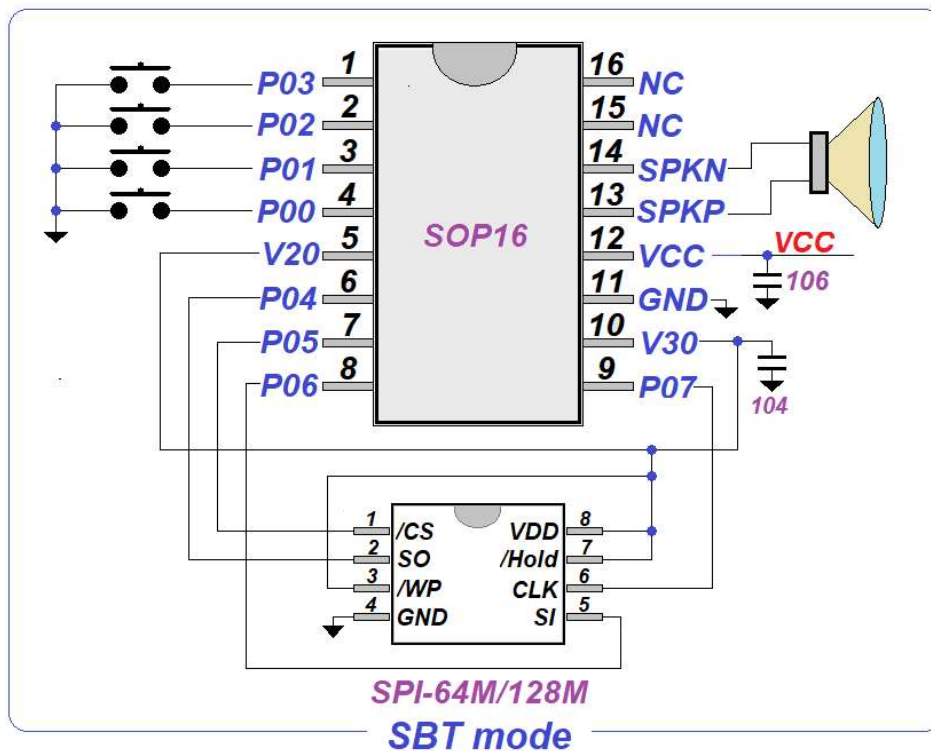
SBT mode has an additional on/off function. (See Fig. 7).

P00	P01	P02	P03
SEQ/VOL/OUT	SEQ/VOL/OUT	SEQ/VOL/OUT	SEQ/VOL/Reset/OUT

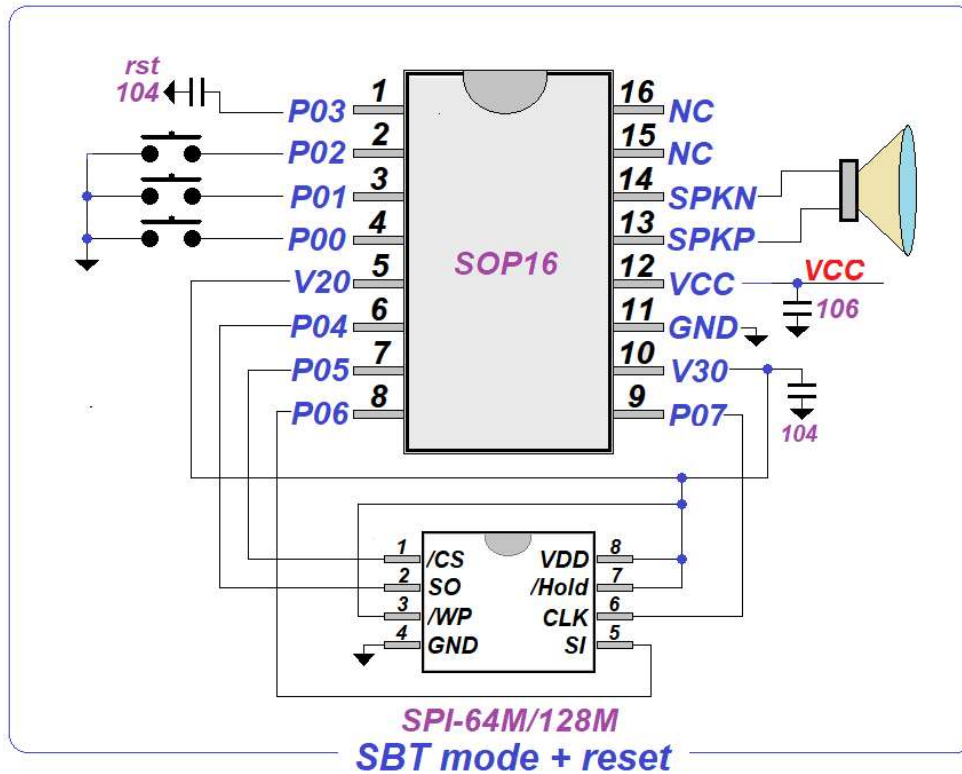
SEQ : Sequential Play (See Fig. 3 and 6).

VOL : Volume Control

Output : BusyH , BusyL , 3Hz , 6Hz , LED-dyna , StopH , StopL



Note : 106 must be connected directly on the VCC and GND pins of the chip.
104 must be connected directly on the V30 and GND pins of the chip.



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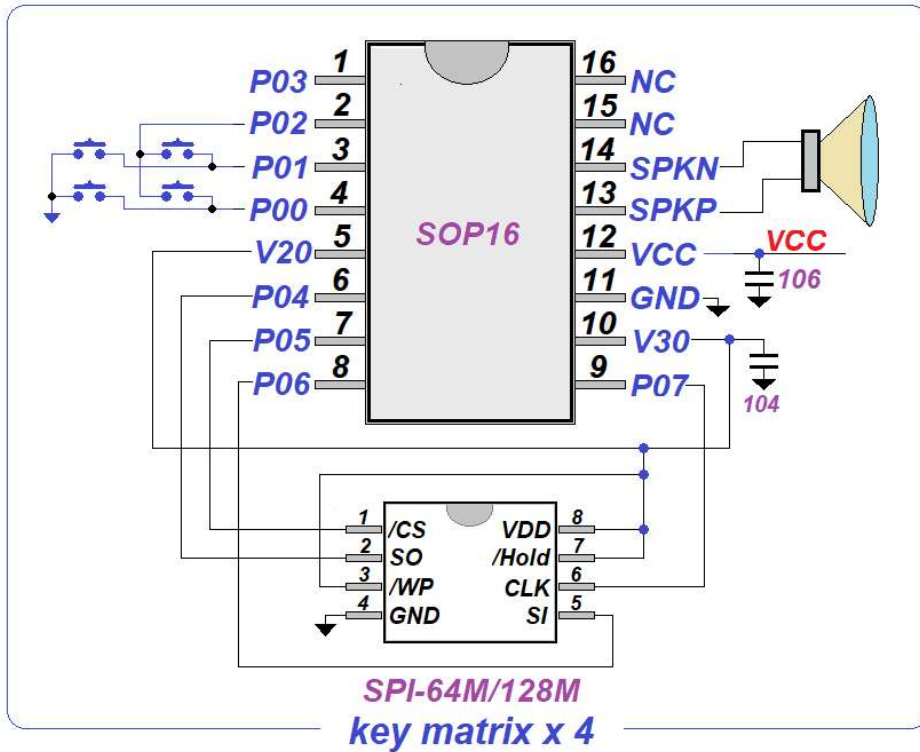
2. Key matrix mode :

The sound group is triggered by combining P00 to P03 and GND in a matrix. All I/O scan is chosen input or output. Each Voice Group can have its independent trigger option (see Figures 1, 2, 4 and 5).

	P00	P01	P02	P03	keyN
4 mkey	scan in	scan in	scan out	Vol/Reset/Out	mkey1~mkey4
6 mkey	scan in	scan in	scan in	scan out	mkey1~mkey6

Output : BusyH , BusyL , 3Hz , 6Hz , LED-dyna , StopH , StopL

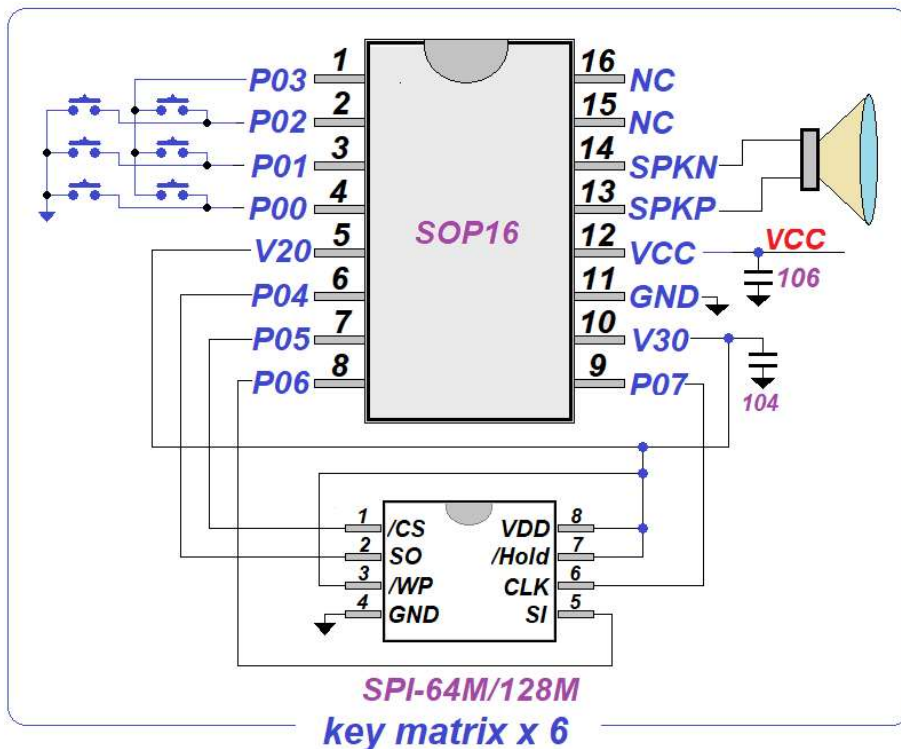
VOL : Volume Control



Ps : p03=input = reset

P03 = output option = busyH , busyL , 3Hz , 6Hz , LED-dyna , stopH , stopL

Note : 106 must be connected directly on the VCC and GND pins of the chip.
104 must be connected directly on the V30 and GND pins of the chip.



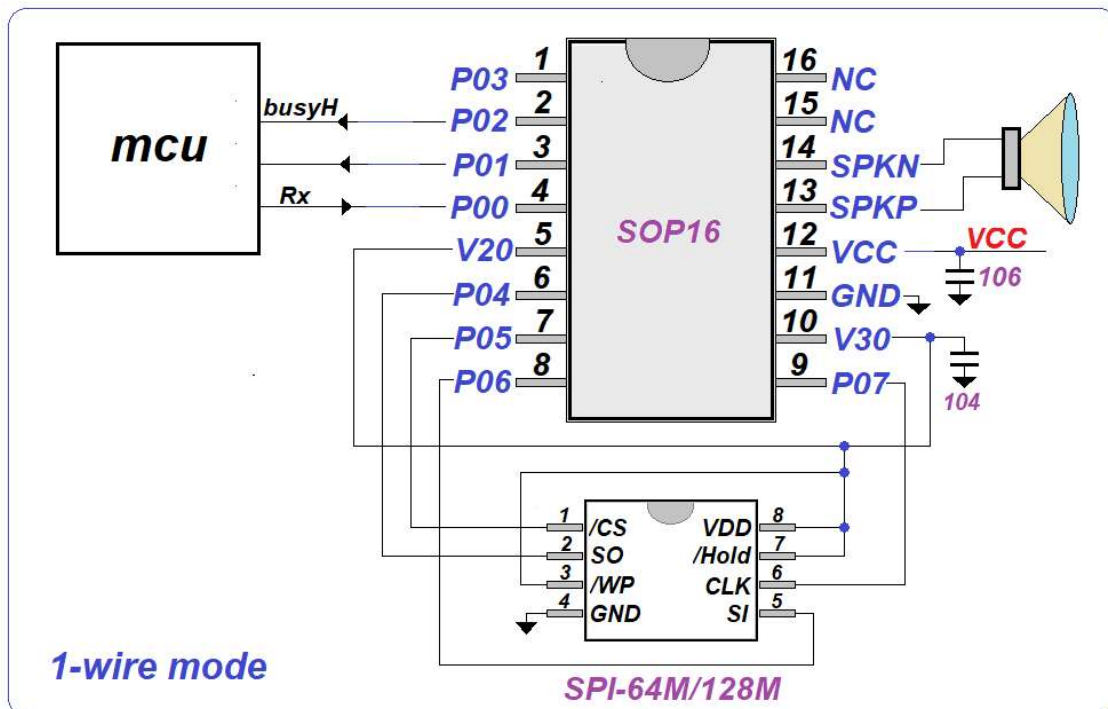
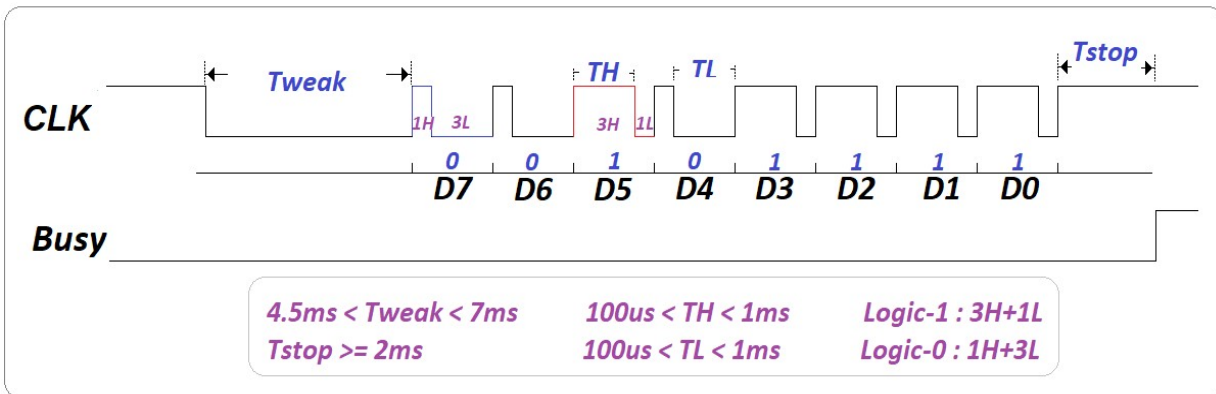
Note : 106 must be connected directly on the VCC and GND pins of the chip.
104 must be connected directly on the V30 and GND pins of the chip.

3. 1-wire mode :

P00	P01	P02	P03
Rx	Out	Out	Out/Reset

Out option : busyH , busyL , 3Hz , 6Hz , LED-dyna , stopH , stopL

P03 = input = reset option



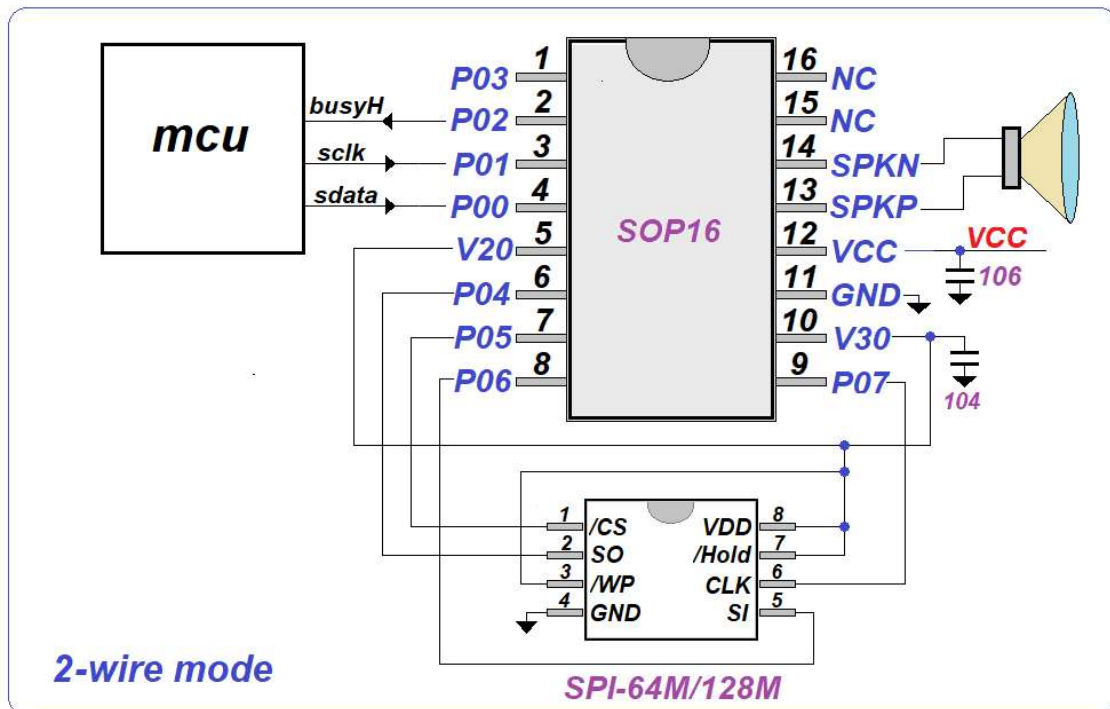
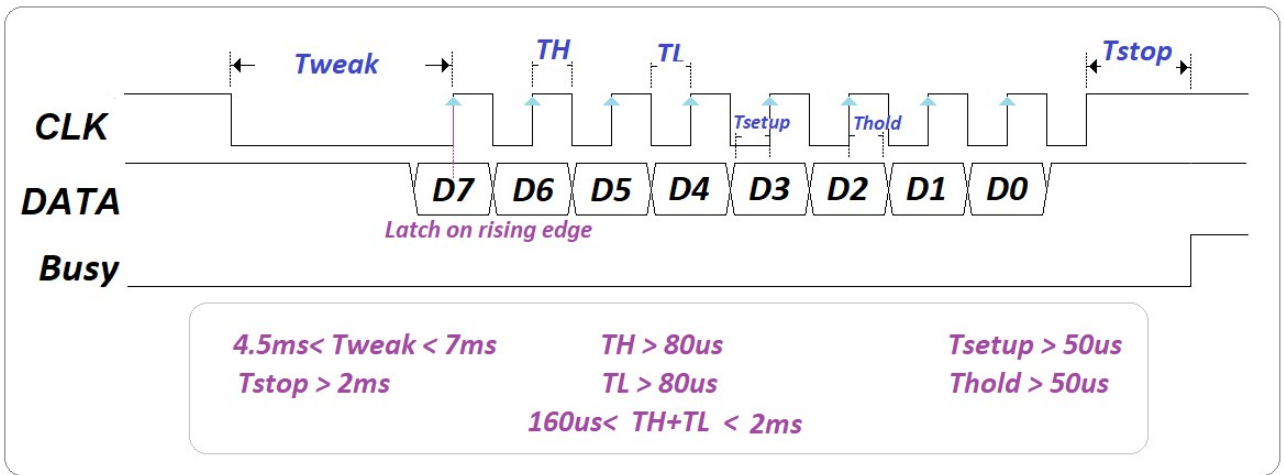
Note : 106 must be connected directly on the VCC and GND pins of the chip.
 104 must be connected directly on the V30 and GND pins of the chip.

4. 2-wire mode :

P00	P01	P02	P03
sdata	sclk	Out	Out/Reset

Out option : busyH , busyL , 3Hz , 6Hz , LED-dyna , stopH , stopL

P03 = input = reset option



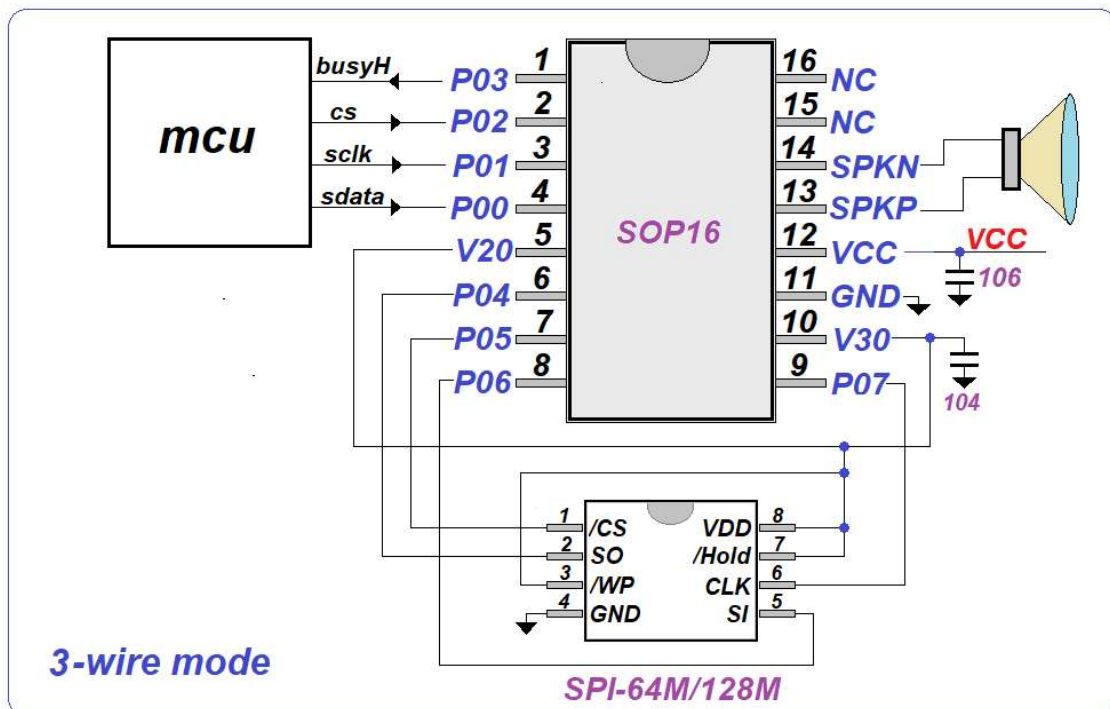
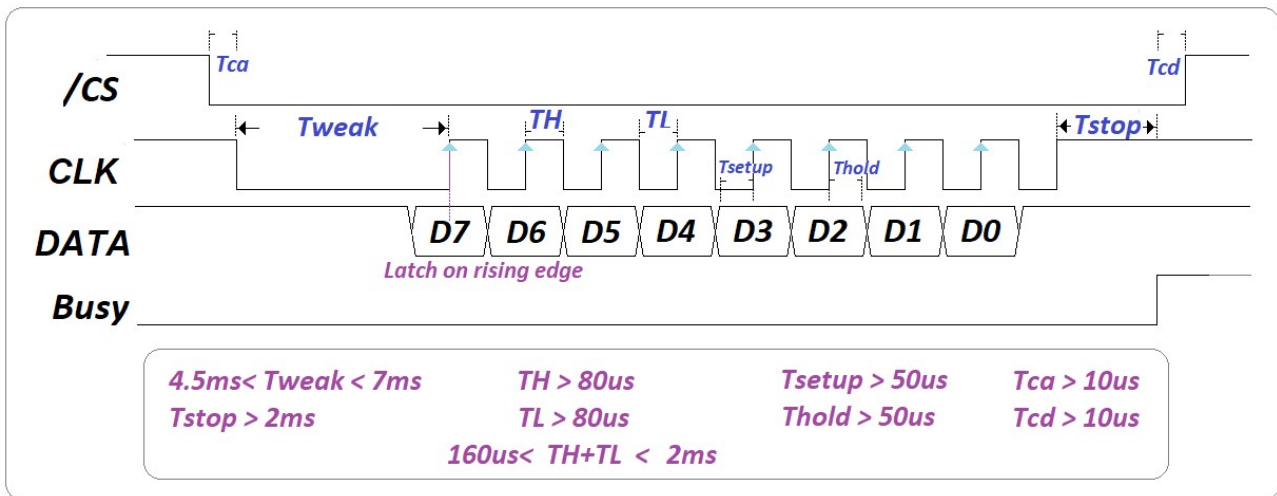
Note : 106 must be connected directly on the VCC and GND pins of the chip.
 104 must be connected directly on the V30 and GND pins of the chip.

5. 3-wire mode :

P00	P01	P02	P03
sdata	sclk	Cs	Out/Reset

Out option : busyH , busyL , 3Hz , 6Hz , LED-dyna , stopH , stopL

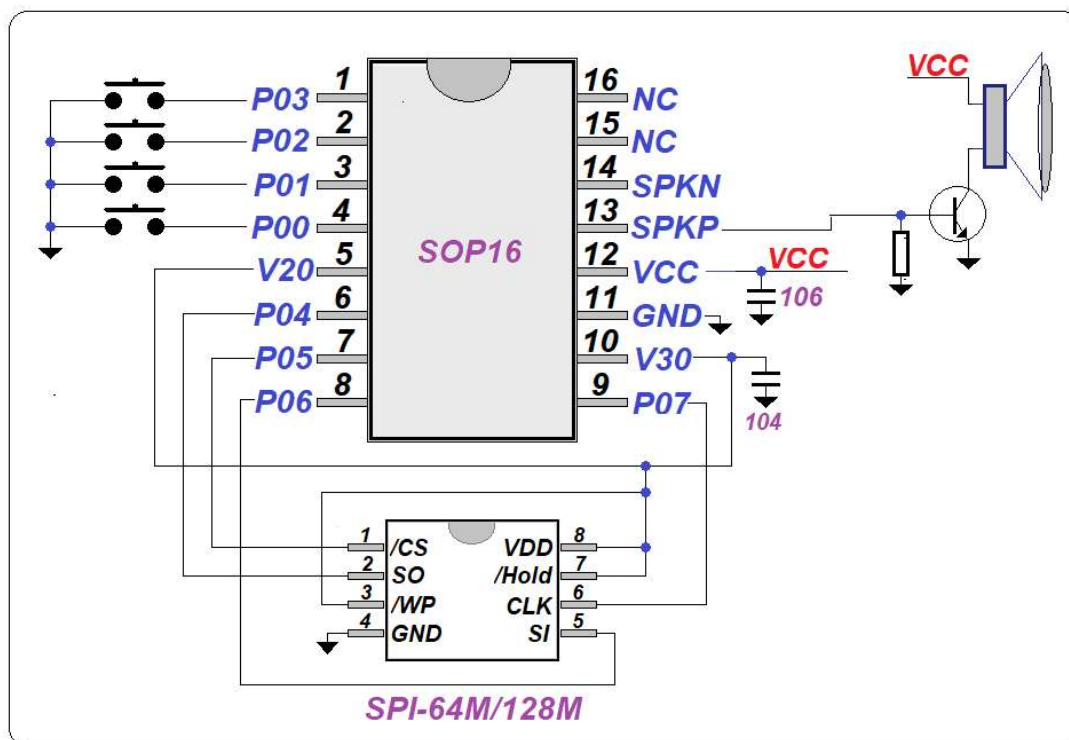
P03 = input = reset option



Note : 106 must be connected directly on the VCC and GND pins of the chip.
 104 must be connected directly on the V30 and GND pins of the chip.

Command :

command	D7	D6	D5	D4	D3	D2	D1	D0
play sentence(n)	01 ~DF							
set volume (n)	E				N (0~15)			
reserved	F0 ~ F7							
repeat off	F8							
repeat on	F9							
Vol-	FA							
Vol+	FB							
Play Next	FC							
Play Next	1	1	1	1	1	1	0	0
Play Previous	FD							
Pause / Resume	FE (Available in PWM mode only)							
Stop	FF							

● DAC Application :


Note : 106 must be connected directly on the VCC and GND pins of the chip.
 104 must be connected directly on the V30 and GND pins of the chip.

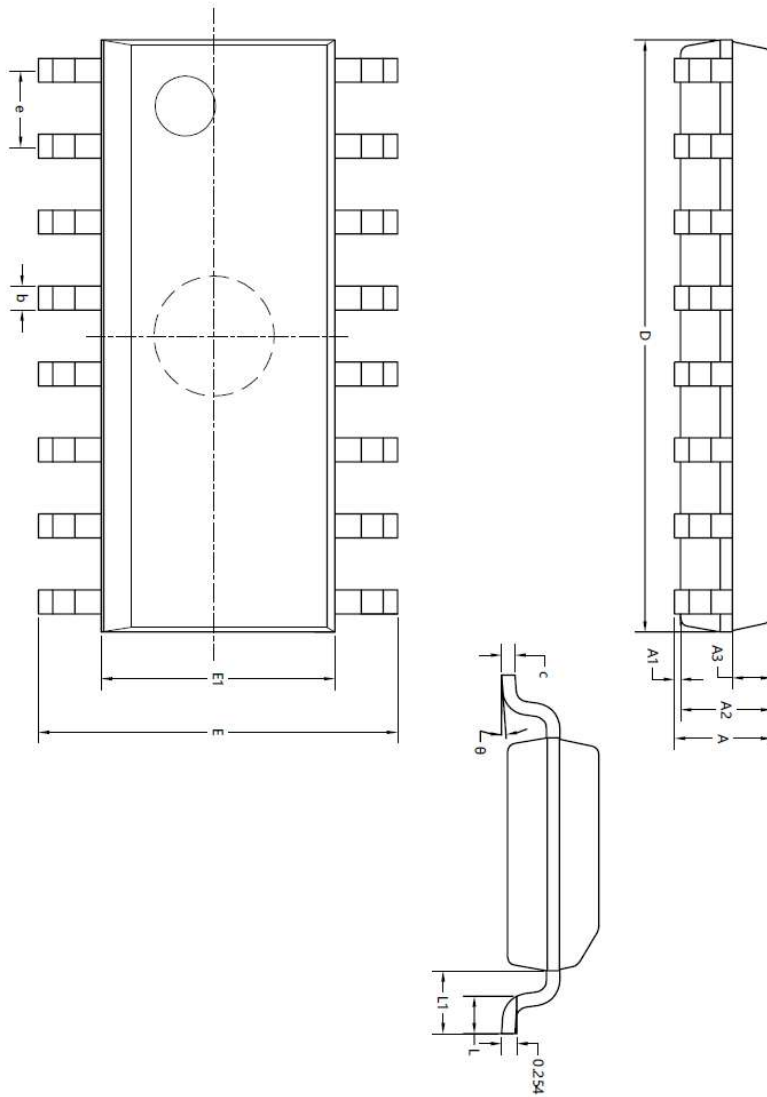
aP58Q7M (64M)					
Coding	AD5	AD6	AD8	PCM10	PCM12
SR = 5.8K	38 min.	31.5 min.	23.5 min.	19 min.	15.5 min.
SR = 6.6K	33 min.	27.5 min.	20.5 min.	16.5 min.	13.5 min.
SR = 7.8K	28.5 min.	23.5 min.	17.5 min.	14 min.	11.5 min.
SR = 9.3K	23.5 min.	19.5 min.	14.5 min.	11.5 min.	9.5 min.
SR = 11.7K	19 min.	15.5 min.	11.5 min.	9.5 min.	7.5 min.
SR = 15.6K	14 min.	11.5 min.	8.5 min.	7 min.	5.5 min.
SR = 23.4K	9.5 min.	7.5 min.	5.5 min.	4.5 min.	3.5 min.

aP58Q8M (128M)					
Coding	AD5	AD6	AD8	PCM10	PCM12
SR = 5.8K	76 min.	63 min.	47 min.	38 min.	31 min.
SR = 6.6K	66 min.	55 min.	41 min.	33 min.	27 min.
SR = 7.8K	57 min.	47 min.	35 min.	28 min.	23 min.
SR = 9.3K	47 min.	39 min.	29 min.	23 min.	19 min.
SR = 11.7K	38 min.	31 min.	23 min.	19 min.	15 min.
SR = 15.6K	28 min.	23 min.	17 min.	14 min.	11 min.
SR = 23.4K	19 min.	15 min.	11 min.	9 min.	7 min.

DC CHARACTERISTICS (VCC = 3.0V , VDD = 2.0V , GND = 0V , TA = 25°C)

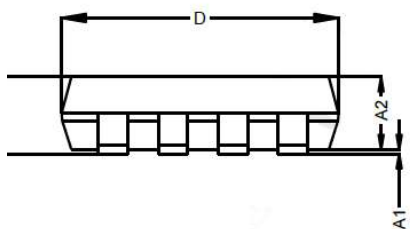
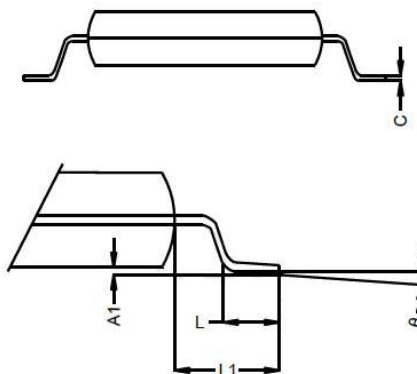
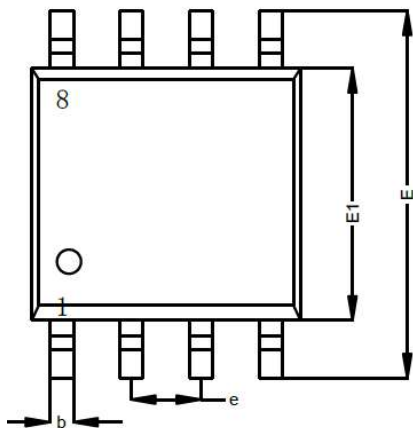
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
PORT0[7:4] PORT0[2:0]	Driving Current(VCC · LDO3V)	1.7		4.8	mA	VOH=2.7
PORT0[3]	Driving Current		1.7		mA	VOH=2.7
SPK_P/SPK_N	Driving Current			200	mA	RL = 8Ω @3.0V
SPK_P/SPK_N	Driving Current			320	mA	RL = 8Ω @4.5V
SPK_P	Current DAC output current			3.52	mA	@4.5V
PORT0[7:4] PORT0[2:0]	Sink Current	2.4		13	mA	VOL=0.3
PORT0[3]	Sink Current		2.5		mA	VOL=0.3
SPK_P/SPK_N	Sink Current			200	mA	RL = 8Ω @3.0V
SPK_P/SPK_N	Sink Current			320	mA	RL = 8Ω @4.5V
I_STD	Standby Current		1	6	uA	<2uA @<4.5V <3uA @4.5~5.1V
V20	output Voltage		2.0		V	
	output Current			60	mA	
	output Current		1		mA	
V30	output Voltage		3.0		V	
	output Current			30	mA	80mA @4.5V
	output Current		1		mA	

▪ aP58HQ package : SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
EI	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

- Flash package : SOP8 (208 mil)



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	2.150
A1	0.050	-	0.250
A2	1.700	-	1.900
b	0.310	-	0.510
c	0.150	-	0.250
D	5.130	5.230	5.330
E	7.800	7.900	8.000
E1	5.180	5.280	5.380
e	-	1.270	-
L	0.500	-	0.800
L1	-	1.310	-
θ	0	-	8°

Note: 1. Dimensions are not to scale

History

23 July 2024

Internal Initial APLUS Release.

01 April 2025

Modify Page.12 Command Table set volume (n) 0E→E

25 May 2026

Modify Page.12 command table.
